A Generalization of Spira's Theorem and Circuits with Small Segregators or Separators

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  Assume fan-in ≤ 2

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- Size: the number of gates
- Depth: length of the longest path from inputs to output

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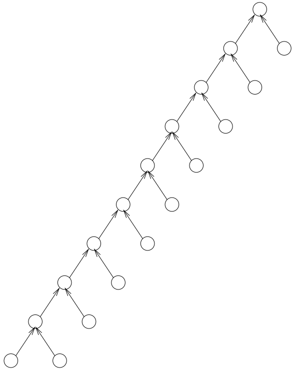

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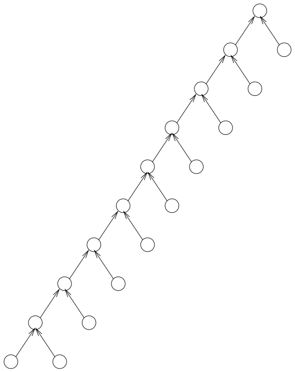

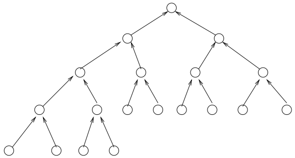

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- Time vs. space: Better general simulation of size by depth in the uniform setting will improve the simulation of (deterministic) *TIME* by *SPACE*.
- Sequential time vs. parallel time: Better general simulation of size by depth will improve the simulation of *TIME* by logcost PRAM.

Separator and Segregator

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- Separator: a subset of nodes whose removal yields two subgraphs of comparable sizes
- Segregator: a relaxed version of separators for DAGs
- Paul, Pippenger, Szemerédi, and Trotter [1983] and Santhanam [2000] used segregators to study the computation graphs of Turing machines

Definition: Separators

Definition

- *A* separator of size k *of a DAG* $G = (V, E)$ *is a set of* k *nodes* $S \subseteq V$ *such that the removal of* S *partitions* $G \setminus S$ *into two subDAGs,* G_1 *and* G_2*, such that* $|G_i| \leq \frac{2}{3}|V|$ *for* $i = 1, 2$*, and there are no edges either from* G_1 *to* G_2*, or from* G_2 *to* G_1 *in* $G \setminus S$*.*

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- *A Boolean circuit C has separators of size $f()$ if the underlying DAG of every subcircuit of C with s gates has a separator of size at most $f(s)$.*

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- Paul, Pippenger, Szemerédi and Trotter [1983]
  A *segregator of size k* of a DAG $G = (V, E)$ is a set of k nodes $S \subseteq V$ such that every node in $G \setminus S$ has at most $\frac{2}{3}|V|$ predecessors in $G \setminus S$.

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Let G be a DAG. If G has a separator of size k, then G also has a segregator of size at most k.

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From now on we focus on segregators.

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- Bonet and Buss [1994] improved the constants in the depth bounds and the size of the simulation for Boolean formulas
- Brent [1974], Bshouty, Cleve, Eberly [1995] extended Spira's theorem to arithmetic formulas
- All these results study formulas, i.e. tree-like circuits with fan-out 1

Recent Advances

Recall:

Theorem

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Boolean circuits with size $n^{O(1)}$ and constant treewidth k can be simulated by circuits of depth $O(k^2 \log n)$, if k and tree-decomposition are given along with circuit description.

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Corollary

Jansen and Sarma [2010]
The class of languages with non-uniform polynomial-size and bounded treewidth circuit families equals non-uniform NC^1.

Our Generalization of Spira's Theorem

Our improvement:

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More generally,

Theorem

Generalization of Spira's Theorem

Any Boolean circuit of size s with segregators of size $f()$ can be simulated in depth $O(f(s)\log s)$. Moreover, if $f(s) = \Omega(s^\epsilon)$ for some constant ϵ, then the simulating circuit has depth $O(f(s))$.

Definition: Uniform Circuit Families

Definition

A family of Boolean circuits $\{C_n\}$ is called h(n)-space uniform, if there exists a deterministic Turing machine M that on input 1^n, outputs the standard description of C_n using space $O(h(n))$ for all n. In particular, $\{C_n\}$ is logspace uniform if $h(n) = \log n$.

Our Result: Uniform Simulation

Theorem

Uniform Generalization of Spira's Theorem

Let

- $\mathcal{C}$: $h(n)$-space uniform family of Boolean circuits
- $C_n \in \mathcal{C}$: has n inputs, size $s = s(n)$, and segregators of size $f()$
- $g(s) = f(s)$ if $f(s) = \Omega(s^c)$ for some constant $c > 0$, and $f(s) \log s$ otherwise

Then $\mathcal{C}$ *can be simulated by a* $O(h(n) + g(s) \log s)$*-space uniform family of Boolean circuits of depth* $O(g(s))$.

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- Our generalization of Spira's theorem is $O(h(n) + g(s) \log s)$-space uniform.
- It is still unknown if Spira's re-structuring algorithm can be done in logspace.

Circuit Value Problem

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- Circuit Value Problem: Given the description of a Boolean circuit C and an input x to C, what is the value of $C(x)$?

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But none of these problems is believed to be P-complete.

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- Goldschlager [1977] Planar Circuit Value is P-complete.
- No sublinear space nor sublinear parallel time algorithm is currently known for CVP over general circuits.

Proofs

Spira's Construction

Lemma

Jordan [1869]

A tree T has a node w whose removal divides T into two subtrees T_1 and T_2, such that the sizes of both subtrees are at most $2/3$ of the size of T.

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Spira's re-structuring formula:

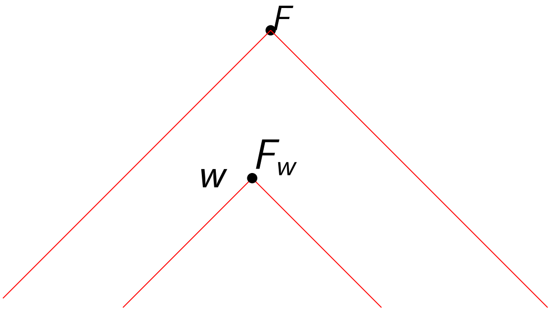
$$F(x) = (F_1(x) \wedge F_w(x)) \vee (F_0(x) \wedge \neg F_w(x)),$$

where w is the node in Jordan's lemma, and

- F_0: function computed by the original formula with w replaced by 0
- F_1: function computed by the original formula with w replaced by 1
- F_w: function computed at w

Spira's Construction

Original circuit:



F: function computed by the circuit

w: separator for the tree

F_w: function computed at w

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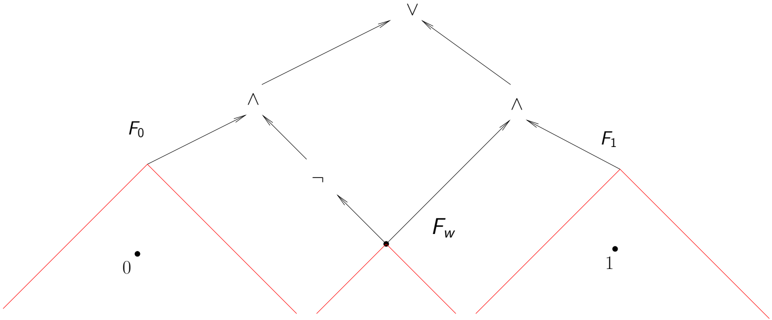
New circuit:



F_0: function computed by the original formula with w replaced by 0

F_1: function computed by the original formula with w replaced by 1

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Proof of Our Generalization of Spira's Theorem

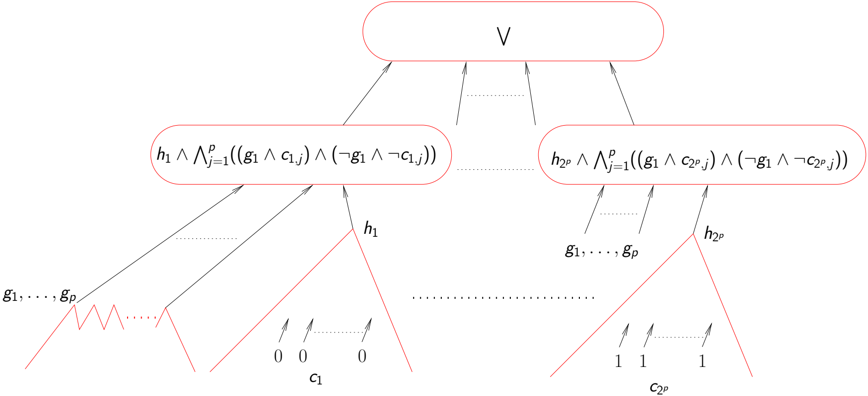
Generalization for circuits with segregators of size $p = f(s)$:

$$\bigvee_{i=1}^{2^p} \left(h_i \wedge \bigwedge_{j=1}^{p} ((g_j \wedge c_{i,j}) \vee (\neg g_j \wedge \neg c_{i,j})) \right),$$

where

- g_j is the function computed at v_j, the jth node in the segregator
- $c_{i,j}$ is the jth bit of the ith Boolean vector of length p $(i = 1 \ldots 2^p)$
- h_i is the function computed by the original circuit after v_j is replaced by $c_{i,j}$ for every $j = 1 \ldots p$

Generalized Construction



p: size of the segregator

c_i: the ith Boolean vector of length p

$c_{i,j}$: the jth component in the ith Boolean vector of length p

h_i: function computed by the original circuit with $v_1, \ldots, v_p$ replaced by c_i

g_i: function computed at v_i

$v_1, \ldots, v_p$: segregator for the circuit

Proof of Uniform Generalization of Spira's Theorem

Recall:

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- $C_n \in \mathcal{C}$*: has n inputs, size $s = s(n)$, and segregators of size $f()$*
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Then $\mathcal{C}$ can be simulated by a $O(h(n) + g(s) \log s)$-space uniform family of Boolean circuits of depth $O(g(s))$.

Outline of Proof

The uniform simulation consists of the following recursive steps.

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Note: The only input is the description of the circuit to be simulated. Size of the minimum segregator is not known in advance.

Generating the Simulating Circuits in Small Space

In each recursive step, perform:

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All can be done in $O(h(n) + f(s) \log s + \log^2 s)$ space

Circuit Value Problem for Circuits with Small Segregators

Theorem

The Circuit Value problem for circuits of size s with segregators of size $f()$ is in $SPACE(f(s)\log s)$ if $f(s) = \Omega(s^{\varepsilon})$ for some constant $\varepsilon > 0$, and $SPACE(f(s)\log^2 s)$ otherwise.

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Follows from

- Our uniform generalization of Spira's Theorem
- Borodin [1977] Any $h(n)$-space uniform circuit family of depth $h(n) \geq \log n$ can be simulated by $O(h(n))$-space Turing machines.

Corollaries

Theorem

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The Planar Circuit Value Problem can be decided in $SPACE(\sqrt{n}\log n)$.

Follows from

- Our theorem in the previous slide
- Lipton and Tarjan [1976] Any planar graph of size s has a separator of size $O(\sqrt{s})$.

Open Questions

- $O(\log s)$ space uniform version of Spira's theorem (Currently we have $O(\log^2 s)$ space uniform)

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- Generate polynomial-size simulating circuits
- Get rid of the $\log s$ factor from the recursion

The End

Savitch's Theorem

Theorem

Savitch [1970]

Given a directed graph G on s nodes and two nodes $u, v \in G$, there exists a deterministic Turing machine that decides if there is a path from u to v in G using space $O(\log^2 s)$.

Find a Minimum Size Segregator in Small Space

For graphs

Lemma

Given: a DAG G with s nodes such that G has a segregator of size $f(s)$
Then: $\exists$ a TM M_1 such that on input G, M_1 outputs a segregator of size at most $f(s)$ using space $O(f(s)\log s + \log^2 s)$.

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Proof Sketch

1. *Given a node v, use Savitch's algorithm to count the number of predecessors of v.*
2. *Enumerate subsets of G in the order of size then in lex. Test if the subset is a segregator by counting the number of predecessors.*

Find a Minimum Size Segregator in Small Space

For uniform circuit families

Lemma

Given:

- $\mathcal{C}$: $h(n)$-space uniform family of circuits
- $C_n \in \mathcal{C}$: size $s = s(n)$ with a segregator of size $\leq f(s)$

Then:

$\exists$ a TM $\hat{M}$ such that on input 1^n, $\hat{M}$ outputs a segregator of C_n of size at most $f(s)$ using space $O(h(n) + f(s) \log s + \log^2 s)$.

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